Unique Paper Code	**: 32341102_OC**	
Name of the Course	**: B.Sc. (H) Computer Science**	
Name of the Paper	**: Computer System Architecture**	
Semester	**: I**	
Duration	**: 3 Hours**	**Maximum Marks: 75**

Instructions for the Candidates

Attempt Any Four Questions. All Questions Carry Equal Marks

Q1.
Given the Boolean function $F = x'y + xyz' + xyz$

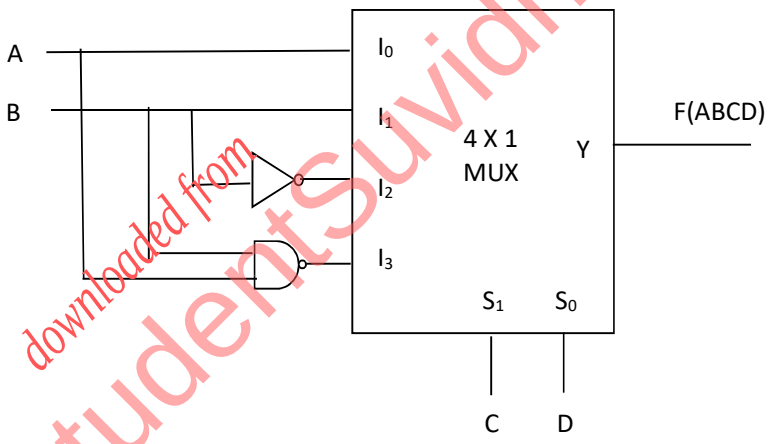
- List the truth table of the function F.
- Draw the logic diagram with NAND gates only.
- Simplify the algebraic expression using Boolean algebra.
- Find complement of the optimized expression F using De-Morgan's Law.

Simplify the Boolean function $f(w,x,y,z) = \sum(0,1,2,3,4,5,8,10)$ with don't care conditions $d(w,x,y,z) = \sum(5,6,11,15)$ using Karnaugh map in

- Sum-of-Products form
- Product-of-Sums form

Q2.
Perform the following operations:

- How many address lines and input-output data lines are needed in $64G \times 32$?
- How many 256×16 memory chips are needed to provide a memory capacity of 8192×32?
- Write the boolean expression for the function F(ABCD) explained by logic circuit shown below.



- Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. The output generates the 1's complement of the input binary number. For example, if input bits are xyz =110, then output bits are ABC =001. Obtain the truth table for all possible combinations of 3-bits. Draw the logic diagram corresponding to each output.
- Represent the hexadecimal number 4F6B2D into binary and octal forms.
- Give decimal representation of $(7982)_{12}$.
- Add two BCD numbers 3456.34 and 0978.45.
- Subtract $(5645)_8$ from $(7056)_8$.

Q3.
Explain briefly what will happen when the following micro instructions are executed:

- $IR \leftarrow M[AR], PC \leftarrow PC + 1$

- $M[AR] \leftarrow PC, PC \leftarrow AR + 1$

Table1 shows the symbolic description of register reference instructions with operation code. The initial value of PC is 025. The content of AC in the basic computer is hexadecimal A789 and the initial value of E is 0.

Table 1. Register-reference Instructions

Symbol	Operation Code	Symbolic Description
CLA	7800	$AC \leftarrow 0$
CMA	7200	$AC \leftarrow \overline{AC}$
CIR	7080	$AC \leftarrow shr\ AC, AC(15) \leftarrow E, E \leftarrow AC(0)$
SPA	7010	$IF(AC(15) = 0)\ then\ PC = PC + 1$
SZA	7004	$IF(AC = 0)\ then\ PC = PC + 1$
SZE	7002	$IF(E = 0)\ then\ PC = PC + 1$

Determine the contents of AC, E, PC, AR, and IR in hexadecimal after the execution of the CLA instruction using given operation code (see Table 1). Repeat the same procedure starting with an operation code (see Table 1) of another register-reference instructions: CMA, CIR, SPA, SZA and SZE.

Q4.
Write a program to evaluate the arithmetic expression $X = (A - B * C)/(D + E)$ using two address instructions.

Consider the following snapshot of memory to answer the following questions.

Address	Memory	
100	306	PC=102
101	104	
102	Mode | AND to AC	XR=205
103	Address = 100	
104	Next instruction	AC=000
	……	
204	762	
205	220	

	……
305	103
306	101

A two-word instruction "AND to AC" being currently executed is stored at location 102 with its address field at location 103. The program counter PC has the value 102 for fetching the instruction. The Accumulator register AC receives the operand after the instruction is executed. An index register XR contains the value 205. Evaluate the effective address and content of AC if the addressing mode of the instruction is:

- Direct
- Immediate
- Indirect
- Relative
- Indexed addressing mode with XR as the index register.

According to general register organizaton of a computer, a 14-bit binary control word consists of three fields SELA, SELB, SELD of 3 bits each, for selecting registers and operation OPR. Specify the control word that must be applied to the processor to implement the following microoperations using Table 2.

- $R2 \leftarrow R1 + R3$
- $R4 \leftarrow R2 \wedge R3$
- $R5 \leftarrow shr\ R5$

Table 2. Encoding of ALU operations

OPR Select	**Operation**
00010	ADD
01000	AND
10000	SHRA

Q5.

A computer uses a memory unit with 1024 words of 32 bits each. One word of memory is used to store a binary instruction code and each instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 30 registers, and an address part.

- How many bits are there in the operation code, the register code and the address part?
- Draw the instruction word format and indicate the number of bits in each part.
- How many bits are there in the data and address inputs of the memory?

Consider a four-segment pipeline to perform the following operations:

- Draw a space-time diagram showing the time it takes to process nine tasks.
- Determine the number of clock cycles that it takes to process 990 tasks.
- A task is processed in a non-pipeline system takes 45ns and the same task can be processed in a pipeline system with a cycle of 15ns. Determine the speedup ratio of the pipeline for 220 tasks.
- What is the maximum speedup that can be achieved?

Q6.

In a DMA controller:

- Why are the read and write control lines bidirectional?

- Under what condition and for what purpose are they used as inputs?
- Under what condition and for what purpose are they used as outputs?

How isolated I/O is different from memory-mapped I/O?

List the advantages and disadvantages of isolated I/O.

Give the excitation table for a flip flop XY whose characteristic table is given as follows:

X	Y	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	?

In the sequential circuit shown below, if the initial value of the output Q_0Q_1 is 11, what are the next four values of Q_0Q_1 ?